

WHAT IS CLAIMED IS:

1. A method for encoding data associated with a page within a non-volatile memory of a memory system, the page having a data area and an overhead area, the method  
5 comprising:  
dividing at least a part of the page into at least two segments of the data, the at least two segments of the data including a first segment and a second segment;  
performing error correction code (ECC) calculations on the first segment to encode the first segment; and  
10 performing the ECC calculations on the second segment to encode the second segment, wherein the second segment is encoded substantially separately from the first segment.
2. The method of claim 1 wherein the first segment includes the data area and the  
15 second segment includes the overhead area.
3. The method of claim 1 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.
- 20 4. The method of claim 1 wherein the ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.
- 25 5. The method of claim 4 wherein the ECC algorithm is a Hamming Code ECC algorithm.
6. The method of claim 1 wherein dividing the at least part of the page into the at least two segments of the data includes:  
dividing the page into three segments, the three segments including the first  
30 segment, the second segment, and a third segment.

7. The method of claim 6 further including:

performing the ECC calculations on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.

8. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.

9. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

10. The method of claim 1 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

11. A memory system comprising:

a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data;

code devices for dividing at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment;

code devices for performing error correction code (ECC) calculations on the first segment to encode the first segment and on the second segment to encode the second segment, wherein the second segment is encoded substantially separately from the first segment; and

a memory area for storing the code devices.

12. The memory system of claim 11 further including:

a controller, the controller being arranged to process the code devices.

13. The memory system of claim 11 wherein the first segment includes the data area and the second segment includes the overhead area.

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14. The memory system of claim 11 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.

15. The memory system of claim 1 wherein the ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.

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16. The memory system of claim 15 wherein the ECC algorithm is a Hamming Code ECC algorithm.

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17. The memory system of claim 11 wherein the code devices for dividing the at least part of the page into the at least two segments include:

code devices for dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.

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18. The memory system of claim 17 further including:

code devices for performing the ECC calculations on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.

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19. The memory system of claim 17 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.

20. The memory system of claim 17 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

5 21. The memory system of claim 11 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

22. The memory system of claim 11 wherein the code devices are one of software code devices and firmware code devices.

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23. A memory system comprising:

a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data;

15 means that divide at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; and

means that perform error correction code (ECC) calculations on the first segment to encode the first segment and on the second segment to encode the second segment, wherein the second segment is encoded substantially separately from the first segment.

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24. The memory system of claim 23 wherein the first segment includes the data area and the second segment includes the overhead area.

25 25. The memory system of claim 23 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.

26. The memory system of claim 1 wherein the ECC calculations are associated with a Hamming Code ECC algorithm that is arranged to correct up to one incorrect bit included in the first segment and up to one incorrect bit included in the second segment.

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27. The memory system of claim 23 wherein the means that divide the at least part of the page into the at least two segments include:

means that divide the page into three segments, the three segments including the first segment, the second segment, and a third segment.

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28. The memory system of claim 27 further including:

means that perform the ECC calculations on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.

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29. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.

15 30. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

31. The memory system of claim 23 wherein the non-volatile memory is one of a  
20 NAND flash memory and an MLC NAND flash memory.